UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/066,019	01/30/2002	Peter Ho	10003431-1	2106

7590 09/23/2005

AGILENT TECHNOLOGIES, INC.
Legal Department, DL429
Intellectual Property Administration
P.O. Box 7599
Loveland, CO 80537-0599

EXAMINER	
TORRES, JUAN A	

ART UNIT	PAPER NUMBER
2631	

DATE MAILED: 09/23/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/066,019	HO ET AL.	
	Examiner	Art Unit	
	Juan A. Torres	2631	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 September 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3-9,12,14-22 and 25-27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3-9,12,14-22 and 25-27* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

The modifications to the specification were received on 09/01/2005. These modifications are accepted by the Examiner.

Claim Objections

In view of the amendment filed on 09/01/2005, the Examiner withdraws claim objections of claim 12 of the previous Office Action.

Response to Arguments

Applicant's arguments filed on 09/01/2005 have been fully considered but they are not persuasive.

Regarding claims 1 and 3-9:

The Applicant contends:

"independent claim 1 was rejected under Claim 1 describes a crosspoint switch integrated circuit. The integrated circuit includes the arrays of input and output ports, the switch matrix, and equalization circuitry. The equalization circuitry of the integrated circuit is configured to measure jitter and to utilize the jitter measurements as the basis for offsetting transmission losses. Applicant assert that McCormack et al. does not teach an Integrated circuit wherein the integrated circuit includes the input and output ports and Includes the equalization circuit configured to measure jitter.

In rejecting claim 2, it was asserted that McCormack et al. discloses equalization circuit configured to measure jitter. The relevant portions of McCormack et al. were cited as being block 201 In Fig. 1 and paragraphs [0008], [0037] and [0054]. In paragraph

[0037], the block 201 is described as being Input signal equalization circuits. There is no Indication that the Input signal equalization circuit should be provided with me capability of measuring jitter. The patent describes access ports (111 and 113) that allow input of programming via a programming interface (109). However block 201 is not identified as being configured to measure jitter. In the cited paragraph on page 1 of McCormack et al. (i.e., paragraph [0008]), it Is merely stated that data degradation may occur due to intersymbol interference (ISI). An explanation of ISI is provided, but there is no teaching of equalization circuitry configured to measure jitter or to be automatically responsive to jitter measurements.

Turning to the cited portion of page 4 of McCormack et al. (i.e., paragraph [0054], the prior art reference states that since the passive network includes passive elements, the elements can be segmented and/or programmable. For example, upper metal layers may be changed in order to allow for tuning of a circuit's ISI Jitter characteristics. However, the passive network of passive elements does not anticipate equalization circuitry that is configured to measure jitter or to be responsive to jitter measurements to automatically select levels of equalization.

Applicants assert that amended claim 1 is patentably distinguishable from the teachings of McCormack et al. Moreover, even if one were to modify McCormack et al. in view of the teachings of Yiu, the resulting circuit would not render Applicants' claimed invention unpatentable. Yiu is cited primarily with respect to the teaching of equalization to offset "skin effect." Yiu is cited for disclosing switchable connections arranged in electrical parallel, with the components including an inductor and a resistor. It is not

asserted that Yiu teaches equalization circuitry within the same integrated circuit as arrays of Input and output ports, wherein the equalization circuitry is configured to measure jitter and to be responsive to jitter measurements to automatically select levels of equalization.".

The Examiner disagrees and asserts, as indicated in the previous Office action, McCormack discloses a crosspoint switch integrated circuit comprising an array of input ports (figure 1 block 301 page 2 paragraph [0037]); an array of output ports (figure 1 block 303 page 2 paragraph [0037]); a switch matrix configured to selectively connect the input ports to the output ports for conducting electrical signals therebetween (figure 1 block 101 page 2 paragraph [0037]); and equalization circuitry coupled to at least partially offset transmission losses experienced by the electrical signal while external to the crosspoint switch integrated circuit (figure 1 block 201 page 2 paragraph [0037]) the equalization circuitry is configured to measure jitter within the electrical signals and to utilize jitter measurements as a basis for offsetting the transmission losses, the equalization circuitry being adaptive circuitry enabled to automatically select levels of equalization (figure 1 block 201 page 1 paragraph [0008] page 2 paragraph [0037] and page 4 paragraph [0054]). McCormack states, "one or more switch matrices are coupled together. For instance, outputs of a first switch matrix are coupled to inputs of a second switch matrix and outputs of the second switch matrix are coupled to inputs of a third switch matrix and so on. Similarly, one or more switch matrices are provided on the same printed circuit board" (paragraph [0046]) and that "switch includes a switch core 101, a switch configuration register 103, a staging register 105, and a programming

interface 109. In somewhat more detail, the switch core couples signals from an input bus 301 to an output bus" (paragraph [0037]), so the element 201 is part of the switch core. McCormack also discloses that "For instance, in one embodiment where the network is included in the integrated circuit, by changing upper metal layers on an integrated circuit, the elements of the network are manipulated and thus allowing for easy tuning of a circuit's ISI jitter characteristics" (paragraph [0054]). The equalizer is tunable or adjustable, McCormack discloses that "Also, since the network includes passive elements, these elements can be segmented and/or programmable (i.e., tunable). For instance, in one embodiment where the network is included in the integrated circuit, by changing upper metal layers on an integrated circuit, the elements of the network are manipulated and thus allowing for easy tuning of a circuit's ISI jitter characteristics" (paragraph [0054]). McCormack also discloses the use of active elements in figures 2 and 7. For these reasons and the reason stated en the previous Office Action, the rejection of claims 1 and 3-9 are maintained.

Regarding claims 25-27:

The Applicant contends, "

The combination of McCormack et al. and Yiu does not teach or suggest an integrate circuit having equalization circuit that includes a multiplexer connected to receive electrical signals from each Input port, with the multiplexer being operationally associated with a jitter measurement component to enable jitter measurements on a port-by-port basis. Therefore, Applicants submit that claim 25 is patentable over me cited prior art.

The combination of McCormack et al. and Yiu does not teach or suggest a jitter measurement device that includes a phase-locked loop for tracking data transmissions within electrical signals as set forth in claim 25. Nor does the combination of prior art teach or suggest a jitter measurement component that includes a voltage controlled oscillator configured to be responsive to operations of the phase-locked look. Therefore, claim 26 is non-obvious In view of the prior art.

Regarding claim 27, the prior art does not teach or suggest equalization circuit configured to recurrently execute jitter measurements and recurringly execute the responsive selection of the levels of equalization for Individual input ports. It is respectfully submitted that claim 27 Is In an allowable condition. ".

The Examiner asserts that these claims have not been presented previously so arguments to these claims are improper at this point.

Regarding claims 19-22:

The Applicant contends:

"Amended claim 19 describes me method as being one in which equalization is provided for a crosspoint switch formed on an integrated circuit chip. The method includes determining signal characteristics, including providing on-chip measurements of jitter, wherein the jitter is induced by off-chip conditions. Equalization circuitry housed within the crosspoint switch is then set, at least partially based on the on-chip measurements of jitter.

Many of the comments made with regard to the patentability of claim 1 apply equally to the determination of patentability of amended claim 19. The primary reference

to McCormack et al. does not anticipate on-chip measuring of jitter. Therefore, McCormack et al. does not anticipate the method described in claim 19- Moreover, it would not be obvious to modify McCormack et al. to include on-chip measuring of jitter and automated setting of equalization circuitry at least partially based on the on-chip jitter measurements. Yiu does not teach such a modification."

The Examiner disagrees and asserts, as indicated in the previous Office action, McCormack discloses a method of providing equalization for a crosspoint formed on an integrated circuit chip switch (McCormack states, "one or more switch matrices are coupled together. For instance, outputs of a first switch matrix are coupled to inputs of a second switch matrix and outputs of the second switch matrix are coupled to inputs of a third switch matrix and so on. Similarly, one or more switch matrices are provided on the same printed circuit board" (paragraph [0046]) and that "switch includes a switch core 101, a switch configuration register 103, a staging register 105, and a programming interface 109. In somewhat more detail, the switch core couples signals from an input bus 301 to an output bus" (paragraph [0037]), so the element 201 is part of the switch core, he also discloses that "For instance, in one embodiment where the network is included in the integrated circuit, by changing upper metal layers on an integrated circuit, the elements of the network are manipulated and thus allowing for easy tuning of a circuit's ISI jitter characteristics" (paragraph [0054])) comprising determining signal characteristics related to signal transmissions via each of a plurality of ports of the crosspoint switch, including providing on-chip measurements of jitter of electrical signals. wherein said jitter is inducted by off-chip conditions (figure 2 block 21 page 1

paragraph [0011] and page 4 paragraphs [0051] to [0056]. McCormack also discloses that "For instance, in one embodiment where the network is included in the integrated circuit, by changing upper metal layers on an integrated circuit, the elements of the network are manipulated and thus allowing for easy tuning of a circuit's ISI jitter characteristics" (paragraph [0054]). The equalizer is tunable or adjustable, McCormack discloses that "Also, since the network includes passive elements, these elements can be segmented and/or programmable (i.e., tunable). For instance, in one embodiment where the network is included in the integrated circuit, by changing upper metal layers on an integrated circuit, the elements of the network are manipulated and thus allowing for easy tuning of a circuit's ISI jitter characteristics" (paragraph [0054]).); and setting equalization circuitry housed within the crosspoint switch such that each the port has filtering characteristics tailored on a basis of the signal characteristics for the signal transmissions via the each port, the settings being automated and being at least partially based on the on-chip measurements of jitter (figure 2 block 21 page 4 paragraphs [0051] to [0056]).The respond to arguments to claims 1 apply to claim 19-22. In addition the specification doesn't disclose what off-chip conditions are, so there is not written description that enable what "said jitter is induced by off-chip conditions". For these reasons and the reason stated en the previous Office Action, the rejection of claims 19-22 are maintained.

Regarding claims 12 and 14-18:

The Applicant contends:

"Claim 12 has been amended to describe me crosspoint switching arrangement as being an integrated circuit having the input ports, the output ports, the switching matrix and the equalization circuitry. Re equalization circuitry of the Integrated circuit includes a separate equalization circuit for each channel for which equalization is to be applied. As set for in claim 12, "channels" are connected to the input ports and *channels* are connected lo the output port. For example, the channels connected to the input ports have non-uniform frequency responses with respect to incoming signal transmissions.

McCormack et al. does not anticipate an integrated circuit that includes equalization circuitry to establish filtering characteristics tailored on the basis of frequency responses of channels that are external to the integrated circuit. McCormack et al. teaches a crosspoint switch unit that Includes internal first transmission lines and internal second transmission lines that are orthogonal to the first transmission lines. A switch matrix determines the connection of the first internal transmission lines to the second internal transmission lines. Prior to the first transmission lines, the crosspoint switch unit includes a passive network of capacitors and resistors to compensate for signal degradation. In paragraph [0019], McCormack et al. states en "general terms the present invention provides a passive network within a signal path before a chain of amplifiers. The passive network has frequency characteristics approximate the inverse of the gain versus the frequency response of the chain of amplifiers over the region that is causing ISI". Applicants submit that the only references to providing compensation for signal degradation that is generated by forces external to the crosspoint switch unit are

those involving the location of circuitry external to the crosspoint switches. Thus, paragraph [0055] teaches that if there are multiple stages of crosspoint switches, a passive network of elements may be placed between each of the cascaded crosspoint switch devices in order to reduce signal degradation. This is consistent with [0053] in which it is stated that the passive network may be applied externally to the Integrated circuit In order to remove ISI already in fabricated circuits.

In the Section 103(a) rejection, Yiu was cited for teaching the equalization of the frequency response of a transmission line. However, even if one were to modify the teachings of McCormack et al. in view of Yiu, the passive network of capacitors and resistor would continue to be placed between the crosspoint switches as taught by McCormack. The teachings of Yiu do not relate to the positioning of circuitry relevant to a switching matrix, of the type described in McCormack et al. or claimed in the pending claims.

Figs. 3. 4A and 8 of Yiu are cited as being relevant. In Fig. 3, a single transmission line is shown. The transmission line is located between a transmitter and a receiver. For purposes of explanation, the transmission line frequency response is modeled by a number of "tapes" (36, 42 and 48). These taps of the transmission lines do not teach or suggest the equalization circuitry or teach a modification of the teachings of McCormack et al. In Fig. 4A, there is a representation of a transfer function which is the inverse of the transmission line transfer function. As described in column 6, lines 27-45 of Yiu, an equalizer may include a number of "taps" that are equivalent to the "taps" of the transmission line as shown in Fig. 3. The number of parallel taps

shown in Fig. 8 and the values of the components within each tap depend upon the frequency range mat Is of Interest and the degree of accuracy mat is desired. In general, the greater the frequency range and the greater the accurate, the greater the number of taps that are required. The taps are described as signal processor circuits which each take me input signal from the transmission line and process the signal to mimic a term In the transfer function (column 5, line 58 to column 6, line 2). The signals from the collection of processors/taps are summed and then multiplied by a programmable gain term. Then, the input is added to the output of the multiplier to form an output equalizer signal.

Applicants submit that it would not be obvious to modify McCormack et al. in view of Yiu, since providing the multiple taps (i.e., signal processors) for summing. as shown in Fig. 8. would be cost and space prohibitive if the group of taps needed to be duplicated for each input transmission line of an Integrated circuit crosspoint switch.".

The Examiner disagrees and asserts, as indicated in claim 1 and in the previous Office action, McCormack states, "one or more switch matrices are coupled together. For instance, outputs of a first switch matrix are coupled to inputs of a second switch matrix and outputs of the second switch matrix are coupled to inputs of a third switch matrix and so on. Similarly, one or more switch matrices are provided on the same printed circuit board" (paragraph [0046]) and that "switch includes a switch core 101, a switch configuration register 103, a staging register 105, and a programming interface 109. In somewhat more detail, the switch core couples signals from an input bus 301 to an output bus" (paragraph [0037]), so the element 201 is part of the switch core. The

discussion should be focus in the claims of the application. For these reasons and the reason stated en the previous Office Action, the rejection of claims 12 and 14-18 are maintained.

Claim Objections

Claim 12 is objected to because of the following informalities: in line 18 of claim 12 the recitation "ports are [connected.] connected, each" is improper; it is suggested to be changed to" ports are connected, each". Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 19-22 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. The specification doesn't disclose that "the jitter is induced by off-chip conditions".

Claim 27 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

The specification doesn't disclose that "recurringly execute said jitter measurement and recurringly execute responsive selection of said levels of equalization".

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1, 3-6, 8, 9, 12, 14, 19, 20 and 22 are rejected under 35 U.S.C. 102(e) as being anticipated by McCormack (US Patent Publication 20020020905 A1).

As per claim 1 McCormack discloses a crosspoint switch integrated circuit comprising an array of input ports (figure 1 block 301 page 2 paragraph [0037]); an array of output ports (figure 1 block 303 page 2 paragraph [0037]); a switch matrix configured to selectively connect the input ports to the output ports for conducting electrical signals therebetween (figure 1 block 101 page 2 paragraph [0037]); and equalization circuitry coupled to at least partially offset transmission losses experienced by the electrical signal while external to the crosspoint switch integrated circuit (figure 1 block 201 page 2 paragraph [0037]) the equalization circuitry is configured to measure jitter within the electrical signals and to utilize jitter measurements as a basis for offsetting the transmission losses, the equalization circuitry being adaptive circuitry

enabled to automatically select levels of equalization (figure 1 block 201 page 1 paragraph [0008] page 2 paragraph [0037] and page 4 paragraph [0054]).

As per claim 3 McCormack discloses the equalization circuitry includes a plurality of adjustable equalizers, the adjustable equalizers each having adjustable filtering characteristics within a fixed number of equalization settings (figure 2 block 21 page 4 paragraphs [0051] to [0056]).

As per claim 4 McCormack discloses that each the adjustable equalizer includes a plurality of switchable connections which individually adjust the filtering characteristics when activated (figure 4 page 4 paragraph [0057]).

As per claim 5 McCormack discloses that each the switchable connection includes a switch, at least some of the switchable connections including at least one component which significantly affects the filtering characteristics when the switchable connections are individually activated (figure 4 page 4 paragraph [0057]).

As per claim 6 McCormack discloses that at least some of the switchable connections are arranged in electrical parallel and the components include capacitors and resistors (figure 4 page 4 paragraph [0057]).

As per claim 8 McCormack discloses that the switches are transistors and the components include at least some of resistors, capacitors, or inductors (figure 4 page 4 paragraph [0057]).

As per claim 9 McCormack discloses that the adjustable equalizers are coupled to the input ports in one-to-one correspondence (figure 2 block 21 page 4 paragraphs [0051] to [0056] and figure 4 page 4 paragraph [0057]).

As per claim 12 McCormack discloses a crosspoint switching arrangement comprising a plurality of input ports connected to channels having non-uniform frequency responses with respect to incoming signal transmissions (figure 1 block 301 page 2 paragraph [0037]); a plurality of output ports connected to channels having non-uniform frequency responses with respect to outgoing signal transmissions (figure 1 block 303 page 2 paragraph [0037]); a switch matrix enabled to dynamically reconfigure connections of the input ports to the output ports (figure 1 block 101 page 2 paragraph [0037]); and equalization circuitry coupled to one of the input and output ports, the equalization circuitry including a separate equalization circuit for each channel for which equalization is to be applied, each equalization circuit having a plurality of available configurations of equalization, where selection of one of the available configurations for a particular equalization circuit establishes (figure 2 paragraphs [0049]-[0056] and figure 4 page 4 paragraph [0057]) filtering characteristics that are tailored on a basis of the frequency responses of the channels to which the specific ones of the input and output ports are connected, each equalization circuit being dedicated to a particular channel (figure 1 block 201 page 2 paragraph [0037]; figure 2 paragraphs [0049]-[0056] and figure 4 page 4 paragraph [0057]);where said crosspoint switching arrangement is an integrated circuit having input ports, output ports, switch matrix and equalization circuit (paragraphs [0037], [0046] and [0054]).

As per claim 14 McCormack discloses a memory configured to store equalization settings for the equalization circuitry, the equalization settings stored at the memory

including a selection of a particular available the configuration for each the equalization circuit (figure 4 page 4 paragraph [0057] and [0060]).

As per claim 19 McCormack discloses a method of providing equalization for a crosspoint formed on an integrated circuit chip switch comprising determining signal characteristics related to signal transmissions via each of a plurality of ports of the crosspoint switch (figure 2 block 21 page 1 paragraph [0011] and page 4 paragraphs [0051] to [0056]), including providing on-chip measurements of jitter of electrical signals, (figure 2 block 21 page 1 paragraph [0011] and page 4 paragraphs [0051] to [0060]), where the jitter is induced by off-chip conditions (figure 2 block 21 page 1 paragraph [0011] and page 4 paragraphs [0053] and [0051] to [0056]); and setting equalization circuitry housed within the crosspoint switch such that each the port has filtering characteristics tailored on a basis of the signal characteristics for the signal transmissions via the each port the setting being automated and being at least partially based on on-chip measurements of jitter(figure 2 block 21 page 4 paragraphs [0051] to [0060]).

As per claim 20 McCormack discloses selectively activating and deactivating switching devices which introduce parallel connections of resistances and capacitances within the adjustable equalization circuitry, the equalization circuitry being a plurality of adjustable equalization circuits (figure 4 page 4 paragraph [0057]).

As per claim 22 McCormack discloses activating adaptive equalization circuitry (figure 2 block 21 page 4 paragraphs [0051] to [0056]).

As per claim 25 McCormack discloses claim 1 McCormack also discloses that the equalization circuit includes a multiplexer connected to a jitter measurement component for providing said jitter measurements, said multiplexer being connected to receive said electrical signals from each of said input ports and being operatively associated with said jitter measurement component to enable the jitter measurement on a port-by-port basis (figure 11 paragraph [0080]-[0084]. The use of multiplexer is also admitted prior art in the specification see [0002] and [0010]).

As per claim 27 McCormack discloses claim 1 McCormack also discloses that the equalization circuit is configured to recurringly execute jitter measurements and recurringly execute responsive selection of levels of equalization for individual input ports, enabling levels of equalization to track variations in transmission losses (figure 2 block 21 and figure 4 paragraphs [0054] to [0057]).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 7, 15-18 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over McCormack (US Patent Publication 20020020905 A1) as applied to claims 5, 12, 15-19 above, and further in view of Yiu (US 6104750 A).

As per claim 7 McCormack discloses claim 5. McCormack discloses that the tap, therefore, includes a capacitance and inductance (page 3 paragraph [0044]).

McCormack doesn't disclose that the switchable connections are arranged in electrical parallel and the components include an inductor and a resistor. Yiu discloses that the switchable connections are arranged in electrical parallel and the components include an inductor and a resistor (figures 3 and 8 column 6 lines 27-45). McCormack and Yiu are analogous art because they are from the same field of endeavor. At the time of the invention, it would have been obvious to a person of ordinary skill in the art to combine in equalized switching matrix disclosed by McCormack the skin effect disclosed by Yiu. The suggestion/motivation for doing so would have been to provide equalizing the frequency response of a transmission line is provided (Yiu abstract). Therefore, it would have been obvious to combine McCormack with Yiu to obtain the invention as specified in claim 7.

As per claim 15 McCormack discloses claim 12. McCormack discloses that each the equalization circuit includes a default configuration of first connected circuit components and a plurality of alternative configurations, the default configuration achieving a first level of frequency-dependent compensation (figure 2 block 21 page 4 paragraphs [0051] to [0056]). McCormack doesn't disclose the compensation for effects of skin loss in signals conducted via the channels. Yiu discloses the compensation for effects of skin loss in signals conducted via the channels (figure 4A column 4 line 66 to column 5 line 8). McCormack and Yiu are analogous art because they are from the same field of endeavor. At the time of the invention, it would have been obvious to a person of ordinary skill in the art to combine in equalized switching matrix disclosed by McCormack the skin effect disclosed by Yiu. The suggestion/motivation for doing so

would have been to provide equalizing the frequency response of a transmission line is provided (Yiu abstract). Therefore, it would have been obvious to combine McCormack with Yiu to obtain the invention as specified in claim 15.

As per claim 16 McCormack and Yiu disclose claim 15. Yiu also discloses that each of the alternative configuration introduces second connected circuit components to achieve different levels of frequency-dependent compensation for the effects of skin loss (figure 4A and figures 3 and 8 column 4 line 66 to column 5 line 8 and column 6 lines 27-45). McCormack and Yiu are analogous art because they are from the same field of endeavor. At the time of the invention, it would have been obvious to a person of ordinary skill in the art to combine in equalized switching matrix disclosed by McCormack the skin effect disclosed by Yiu. The suggestion/motivation for doing so would have been to provide equalizing the frequency response of a transmission line is provided (Yiu abstract). Therefore, it would have been obvious to combine McCormack with Yiu to obtain the invention as specified in claim 16.

As per claim 17 McCormack and Yiu disclose claim 16. McCormack also discloses that the second connected circuit components are coupled to switches that selectively introduce the second connected circuit components, the switches being manipulated based upon the equalization settings stored in the memory (figure 4 page 4 paragraph [0057]). McCormack and Yiu are analogous art because they are from the same field of endeavor. At the time of the invention, it would have been obvious to a person of ordinary skill in the art to combine in equalized switching matrix disclosed by McCormack the skin effect disclosed by Yiu. The suggestion/motivation for doing so

would have been to provide equalizing the frequency response of a transmission line is provided (Yiu abstract). Therefore, it would have been obvious to combine McCormack with Yiu to obtain the invention as specified in claim 17.

As per claim 18 McCormack and Yiu disclose claim 17. McCormack also discloses that the equalization circuits are coupled to the input ports and are individually adjustable from an exterior of an integrated circuit chip package in which the equalization circuits and switch matrix reside (figure 2 block 21 page 4 paragraphs [0051] to [0056]). McCormack and Yiu are analogous art because they are from the same field of endeavor. At the time of the invention, it would have been obvious to a person of ordinary skill in the art to combine in equalized switching matrix disclosed by McCormack the skin effect disclosed by Yiu. The suggestion/motivation for doing so would have been to provide equalizing the frequency response of a transmission line is provided (Yiu abstract). Therefore, it would have been obvious to combine McCormack with Yiu to obtain the invention as specified in claim 18.

As per claim 21 McCormack discloses claim 19. McCormack discloses selectively activating and deactivating switching devices (figure 4 page 4 paragraph [0057]). McCormack doesn't disclose series connections of resistances and inductances within the adjustable equalization circuits. Yiu discloses series connections of resistances and inductances within the equalization circuits (figures 3 and 8 column 6 lines 27-45). McCormack and Yiu are analogous art because they are from the same field of endeavor. At the time of the invention, it would have been obvious to a person of ordinary skill in the art to combine in equalized switching matrix disclosed by

McCormack the skin effect disclosed by Yiu. The suggestion/motivation for doing so would have been to provide equalizing the frequency response of a transmission line is provided (Yiu abstract). Therefore, it would have been obvious to combine McCormack with Yiu to obtain the invention as specified in claim 21.

Claim 26 is rejected under 35 U.S.C. 103(a) as being unpatentable over McCormack (US Patent Publication 20020020905 A1) as applied to claim 25 above, and further in view of Blazo (US 5757652 A). McCormack discloses claim 25. McCormack doesn't disclose a jitter measurement component includes a phase-locked loop for tracking data transactions within electrical signals, the jitter measurement component including a voltage-controlled oscillator connected to be responsive to operations of the phase locked loop. Blazo discloses a jitter measurement component includes a phase-locked loop for tracking data transactions within electrical signals, the jitter measurement component including a voltage-controlled oscillator connected to be responsive to operations of the phase locked loop (figure 1 column 3 lines 36-50). McCormack and Blazo are analogous art because they are from the same field of endeavor. At the time of the invention, it would have been obvious to a person of ordinary skill in the art to combine in equalized switching matrix disclosed by McCormack the jitter measurement circuit disclosed by Blazo. The suggestion/motivation for doing so would have been to measure jitter at low frequencies (Blazo abstract and lines 36-50). Therefore, it would have been obvious to combine McCormack with Blazo to obtain the invention as specified in claim 25.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Ducaroir (US 6331999 B1) discloses a serial data transceiver architecture and test method for measuring the amount of jitter within a serial data stream using a PLL with VCO (figure 4 column 7 lines 30-67).

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Juan A. Torres whose telephone number is (571) 272-3119. The examiner can normally be reached on Monday-Friday 9:00 AM - 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mohammad H. Ghayour can be reached on (571) 272-3021. The fax phone

number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Juan Alberto Torres
09-20-2005

KEVIN BURD
PRIMARY EXAMINER